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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 10001834-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	**Rex Petersen et al.**		
Serial No.:	**09/510,974**	**Examiner:**	**S. Whitmore**
Filing Date:	**February 21, 2000**	**Group Art Unit:**	**2812**
Title:	**RESISTANCE AND CAPACITANCE ESTIMATION**		

Commissioner for Patents
Washington, D.C. 20231

AMENDMENT

Sir:

In response to the Office Action mailed January 18, 2002, Applicants respectfully request that the Examiner reconsider the application in view of the amendments and comments set forth below.

In the Claims

Pursuant to 37 C.F.R. §1.121(c)(1), Applicants have set forth amendments to the claims by rewriting claims 1, 7-8, 11, and 17-18 with all changes. Applicants have submitted new claim 21 for consideration. Applicants have included all pending claims, whether amended or unchanged, for the convenience of the Examiner. Also, Applicants have submitted in a separate paper, a marked up version of claims 1, 7-8, 11, and 17-18, showing the amendments to claims 1, 7-8, 11, and 17-18.

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A1

1. (Amended) A method for VLSI chip design comprising the steps of:
estimating signal routes between functional blocks;
determining resistance and capacitance values for the estimated signal routes; and
building a model of said signal routes including resistance and capacitance values.

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